LESSON PLAN	
GP MAYURBHANJ	
AcademicYear:**2026-2027**	Name of the Faculty:**JOGESWAR NAIK** **(Lecturer Stage-II) E & TC**
Course name: **Digital Electronics and Microprocessor (TH-1)**	CourseNo.:**EEPC301**
Branch: **Electrical**	Program: **Diploma**
Section:**NA**	Year/Sem:**3rd/5th**

Sl. No.	Period	Time (min)	Teaching Method	Topic to be Covered	Unit
1.	1.	60 min	Black board	Digital Fundamentals Number Systems – Decimal, Binary, Octal, Hexadecimal	**I**
2.	2.	60 min	Black board	1‘s and 2‘s complements	**I**
3.	3.	60 min	Black board	Codes – Binary, BCD,	**I**
4.	4.	60 min	Black board	Excess 3, Gray, Alphanumeric codes	**I**
5.	5.	60 min	Black board	Boolean theorems	**I**
6.	6.	60 min	Black board	Logic gates and truth tables	**I**
7.	7.	60 min	Black board	Universal gates, Sum of products and product of sums	**I**
8.	8.	60 min	Black board	Minterms and Maxterms, Karnaugh map Minimization and QuineMcCluskey method of minimization	**I**
9.	9.	60 min	Black board	Combinational & Synchronous Sequential Circuits Design of Half and Full Adders	**II**
10.	10.	60 min	Black board	Half and Full Subtractors	**II**
11.	11.	60 min	Black board	Binary Parallel Adder -Multiplexer, Demultiplexers	**II**
12.	12.	60 min	Black board	Decoders, and Priority Encoder	**II**
13.	13.	60 min	Black board	Flip flops – SR	**II**
14.	14.	60 min	Black board	Flip flops – JK	**II**
15.	15.	60 min	Black board	Flip flops – T,D	**II**
16.	16.	60 min	Black board	design of clocked sequential circuits	**II**
17.	17.	60 min	Black board	Design of Counters- Shift registers, Universal Shift Register.	**II**
18.	18.	60 min	Black board	Asynchronous Sequential Circuits And Memory Devices Stable and Unstable states, output specifications	**III**
19.	19.	60 min	Black board	cycles and races, state reduction	**III**
20.	20.	60 min	Black board	race free assignments, Hazards,Essential Hazards	**III**
21.	21.	60 min	Black board	Pulse mode sequential circuits	**III**
22.	22.	60 min	Black board	Design of Hazard free circuits	**III**
23.	23.	60 min	Black board	Basic memory structure – ROM -PROM – EPROM	**III**

24.	24.	60 min	Black board	EEPROM –EAPROM, RAM – Static and dynamic RAM	**III**
25.	25.	60 min	Black board	Programmable Logic Devices, Programmable Logic Array (PLA)	**III**
26.	26.	60 min	Black board	Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA).	**III**
27.	27.	60 min	Black board	8085 Processor Hardware Architecture	**IV**
28.	28.	60 min	Projector	Hardware Architecture	**IV**
29.	29.	60 min	Projector	pin diagram	**IV**
30.	30.	60 min	Projector	pin diagram	**IV**
31.	31.	60 min	Black board	Functional Building Blocks of Processor	**IV**
32.	32.	60 min	Black board	Memory organization	**IV**
33.	33.	60 min	Black board	I/O ports and data transfer concepts	**IV**
34.	34.	60 min	Projector	Timing Diagram	**IV**
35.	35.	60 min	Black board	Interrupts.	**IV**
36.	36.	60 min	Projector	Programming Processor Instruction – format and addressing modes	**V**
37.	37.	60 min	Projector	Assembly language format	**V**
38.	38.	60 min	Projector	Data transfer	**V**
39.	39.	60 min	Black board	data manipulation	**V**
40.	40.	60 min	Black board	control instructions	**V**
41.	41.	60 min	Black board	Programming: Loop structure with counting	**V**
42.	42.	60 min	Black board	Programming: Loop structure with Indexing	**V**
43.	43.	60 min	Black board	Look up table	**V**
44.	44.	60 min	Black board	Subroutine instructions	**V**
45.	45.	60 min	Black board	stack -8255 architecture and operating modes	**V**