GOVT. POLYTECHNIC MAYURBHANJ LESSON PLAN

ACADEMIC SESSION(2024-25)

Discipline : ELECTRICAL ENGG.	Semester: 5th Sem	Name of the Teaching Faculty :Leena Marndi
Subject : DEC&MP	No. of Days / per week class allotted : 05	Semester From date : 01.07.2024 To Date : 08.11.2024

MONTH	Week	Day	Topics
JULY	1st	1st	1.**BASICS OF DIGITAL ELECTRONICS** Binary, Octal, Hexadecimal number systems and compare with Decimal system.
		2nd	Binary addition, subtraction, Multiplication and Division.
		3rd	1.4 Subtraction of binary numbers in 2's complement method.
		4th	Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
		5th	1. Importance of parity Bit. 2.Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	2nd	1st	Realize AND, OR, NOT operations using NAND gates
		2nd	Realize AND, OR, NOT operations using NOR gates
		3rd	Different postulates and De-Morgan's theorems in Boolean algebra.
		4th	Use Of Boolean Algebra For Simplification Of Logic Expression
		5th	Use Of Boolean Algebra For Simplification Of Logic Expression
	3rd	1st	Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
		2nd	Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.

		4th	Revision
		5th	Revision
	4TH	1st	Revision
		2nd	**2. COMBINATIONAL LOGIC CIRCUITS**
		3rd	Half adder circuit and verify its functionality using truth table
		4th	Realize a Half-adder using NAND gates only and NOR gates only.
		5th	Full adder circuit and explain its operation with truth table.
	5TH	1st	Realize full-adder using two Half-adders and an OR – gate and write truth table
		2nd	Full subtractor circuit and explain its operation with truth table.
		3rd	Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
AUGUST	1st	4th	REVISION
		5th	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	2nd	1st	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
		2nd	Working of Two bit magnitude comparator.
		3rd	Working of Two bit magnitude comparator.
		4th	REVISION
		5th	REVISION
	3rd	1st	**3. SEQUENTIAL LOGIC CIRCUITS** 3.1
		2nd	Give the idea of Sequential logic circuits
		3rd	State the necessity of clock and give the concept of level clocking and edge triggering
		5th	**CLASS TEST-1**
	4TH	2nd	Clocked SR flip flop with preset and clear inputs.
		3rd	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
		4th	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
		5th	Concept of race around condition and study of master slave JK flip flop
		2nd	Give the truth tables of edge triggered D and T flip flops and draw their symbols.

	5TH	3rd	Applications of flip flops 3.9 Define modulus of a counter 3.10 4-bit asynchronous counter and its timing diagram
		4th	Asynchronous decade counter.
		5th	3.12 4-bit synchronous counter.
SEPTEMBER	1st	1st	3.13 Distinguish between synchronous and asynchronous counters
		2nd	3.14 State the need for a Register and list the four types of registers.
		3rd	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
		4th	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
		5th	REVISION
	2nd	1st	REVISION
		2nd	**4.8085 MICROPROCESSOR**
		3rd	1. Introduction to Microprocessors, Microcomputers 2.Architecture of Intel 8085A Microprocessor and description of each block.
		4th	Architecture of Intel 8085A Microprocessor and description of each block.
		5th	Pin diagram and description.
	3rd	2nd	Pin diagram and description.
		3rd	Stack, Stack pointer & stack top
		4th	Interrupts
		5th	**INTERNAL**
	4TH	1st	Opcode & Operand,
		2nd	Differentiate between one byte, two byte & three byte instruction with example.
		3rd	Instruction set of 8085 example
		4th	Addressing mode
		5th	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5TH	1st	Timing Diagram for memory read, memory write, I/O read, I/O write
		2nd	Timing Diagram for memory read, memory write, I/O read, I/O write

OCTOBER	1st	4th	Timing Diagram for 8085 instruction
		5th	Timing Diagram for 8085 instruction
	3rd	1st	Counter and time delay.
		2nd	Simple assembly language programming of 8085.
		4th	Simple assembly language programming of 8085.
		5th	REVISION
	4TH	1st	REVISION
		2nd	**5. INTERFACING AND SUPPORT CHIPS**
		3rd	Basic Interfacing Concepts, Memory mapping & I/O mapping
		4th	Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
		5th	Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controlle
	5TH	1st	Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controlle
		2nd	Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controlle
		3rd	REVISION
NOVEMBER	1st	5th	**CLASS TEST-2**
	2nd	1st	REVISION
		2nd	REVISION
		3rd	**SECOND MONTHLY TEST**
		4th	**SECOND MONTHLY TEST**
		5th	REVISION

NO. OF PERIOD=82