GOVT. POLYTECHNIC MAYURBHANJ LESSON PLAN

Discipline : ELECTRICAL		Semester: 5th Sem		Name of the Teaching Faculty :Leena Marndi
Subject : DEC&MP lab		No. of Periods/ per week class allotted : 03*2		Semester From date : 01.07.2024 To Date : 08.11.2024
MONTH	**Week**	**Day**		**Topics**
JULY	1st	3rd		**Digital Electronics**
			G-I	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.
		4th	G-II	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.
	2nd	3rd	G-I	Implement various gates by using universal properties of NAND & NOR gates and verify truth table.
		4th	G-II	Implement various gates by using universal properties of NAND & NOR gates and verify truth table.
	3rd	4th	G-II	Implement half adder and Full adder using logic gates.. Implement half subtractor and Full subtractor using logic gates
	4TH	3rd	G-I	Implement half adder and Full adder using logic gates.. Implement half subtractor and Full subtractor using logic gates
		4th	G-II	Implement a 4-bit Binary to Gray code converter. Implement a Single bit digital comparator
	5TH	3rd	G-I	Implement a 4-bit Binary to Gray code converter. Implement a Single bit digital comparator
AUGUST	1st	4th	G-II	Study Multiplexer and demultiplexer.
	2nd	3rd	G-I	Study Multiplexer and demultiplexer.
		4th	G-II	Study of flip-flops. i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
	3rd	3rd	G-I	Study of flip-flops. i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
	4TH	3rd	G-I	Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting.
				Realize a 4-bit synchronous UP/Down counter with a control for up/down
				Implement Mode-10 asynchronous counters.counting.
				Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting.

		4th	G-II	Realize a 4-bit synchronous UP/Down counter with a control for up/down
				Implement Mode-10 asynchronous counters.counting.
	5TH	3rd	G-I	Study shift registers.
		4th	G-II	Study shift registers.
SEPTEMBER	1st	3rd	G-I	**Microprocessor** , 1. a. 1'S Complement. b. 2'S Complement.
		4th	G-II	1. a. 1'S Complement. b. 2'S Complement.
	2nd	3rd	G-I	2. a. Addition of 8-bit number. b. Subtraction of 8-bit number resulting 8/16 bit number
		4th	G-II	2. a. Addition of 8-bit number. b. Subtraction of 8-bit number resulting 8/16 bit number
	3rd	3rd	G-I	3. a. Decimal Addition 8-bit number. b. Decimal Subtraction 8-bit number
		4th	G-II	3. a. Decimal Addition 8-bit number. b. Decimal Subtraction 8-bit number
	4TH	3rd	G-I	4. a. Compare between two numbers. b. Find the largest in an Array
		4th	G-II	4. a. Compare between two numbers.
OCTOBER	1st	4th	G-II	b. Find the largest in an Array
	3rd	4th	G-II	Block Transfer
	4TH	3rd	G-I	Block Transfer
		4th	G-II	Traffic light control using 8255.
	5TH	3rd	G-I	Traffic light control using 8255.
NOVI	1st	3rd	G-I	Generation of square wave using 8255
		4th	G-II	Generation of square wave using 8255

Total Practical days=31