## GOVT. POLYTECHNIC MAYURBHANJ LESSON PLAN

Discipline : ELECTRICAL ENGG.		Semester: 5th Sem	Name of the Teaching Faculty :Leena Marndi
Subject : DEC&MP		No. of Days / per week class	Semester From date : 01.10.2021 To Date : 08.01.2022
ACADEMIC SESSION:2021-22			
MONTH	Week	Day	Topics
	1st	5TH	BASICS OF DIGITAL ELECTRONICS Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	2nd	1ST	Binary addition, subtraction, Multiplication and Division.
		2ND	Subtraction of binary numbers in 2's complement method.
		4TH	Use of weighted and Un-weighted codes & write Binary equivalent number
		5TH	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
~	3RD	1ST	Realize AND, OR, NOT operations using NAND gates
OCTOBER	4TH	1ST	Realize AND, OR, NOT operations using NOR gates
CTC		4th	Different postulates and De-Morgan's theorems in Boolean algebra.
0		5th	Use Of Boolean Algebra For Simplification Of Logic Expression
	5TH	1st	Use Of Boolean Algebra For Simplification Of Logic Expression
		2ND	Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
		3ED	Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
		4TH	Half adder circuit and verify its functionality using truth table
	1ST	1st	Realize a Half-adder using NAND gates only and NOR gates only.
BER		2nd	Full adder circuit and explain its operation with truth table.
NOVEMBER		3rd	Realize full-adder using two Half-adders and an OR – gate and write truth table
		5TH	Realize full-adder using two Half-adders and an OR – gate and write truth table
	2ND	1st	Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer

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		3RD	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
		4TH	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
		5TH	Working of Two bit magnitude comparator.
		1st	Working of Two bit magnitude comparator.
	200	2nd	Give the idea of Sequential logic circuits
	3RD	3RD	State the necessity of clock and give the concept of level clocking and edge triggering
		4TH	Clocked SR flip flop with preset and clear inputs.
	4ТН	1st	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
		2nd	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
		3RD	Concept of race around condition and study of master slave JK flip flop
		4TH	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
		5TH	Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	5TH	1st	Applications of flip flops
		2ND	4-bit asynchronous counter and its timing diagram
		5th	Asynchronous decade counter.
	1ST	3rd	4-bit synchronous counter.
		4th	Distinguish between synchronous and asynchronous counters
		5th	State the need for a Register and list the four types of registers.
	2ND	1st	Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
		2nd	Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
CEMBER		3RD	Introduction to Microprocessors, Microcomputers
Ŭ E		4TH	Architecture of Intel 8085A Microprocessor and description of each block.
DEC		5TH	Pin diagram and description.
	3RD	1st	Pin diagram and description.
		2nd	Stack, Stack pointer & stack top
		3RD	Interrupts
		4TH	Instruction set of 8085 example
		5TH	Instruction set of 8085 example

1		1st	Addressing mode
	4ТН	2nd	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
		3RD	Timing Diagram for memory read, memory write, I/O read, I/O write
		4TH	Timing Diagram for memory read, memory write, I/O read, I/O write
		5TH	Timing Diagram for 8085 instruction
	5TH	1st	Timing Diagram for 8085 instruction
		2nd	Counter and time delay.
		3RD	Simple assembly language programming of 8085.
		4TH	Simple assembly language programming of 8085.
		5TH	Basic Interfacing Concepts, Memory mapping & I/O mapping
	2ND	1st	interface Intel 8255
K≺		2nd	Application using 8255: Seven segment LED display,
JANUARY		3RD	Square wave generator,
JAN		4TH	Traffic light Controller
		5 <sup>™</sup>	RIVISION

TOTALCLASS=62